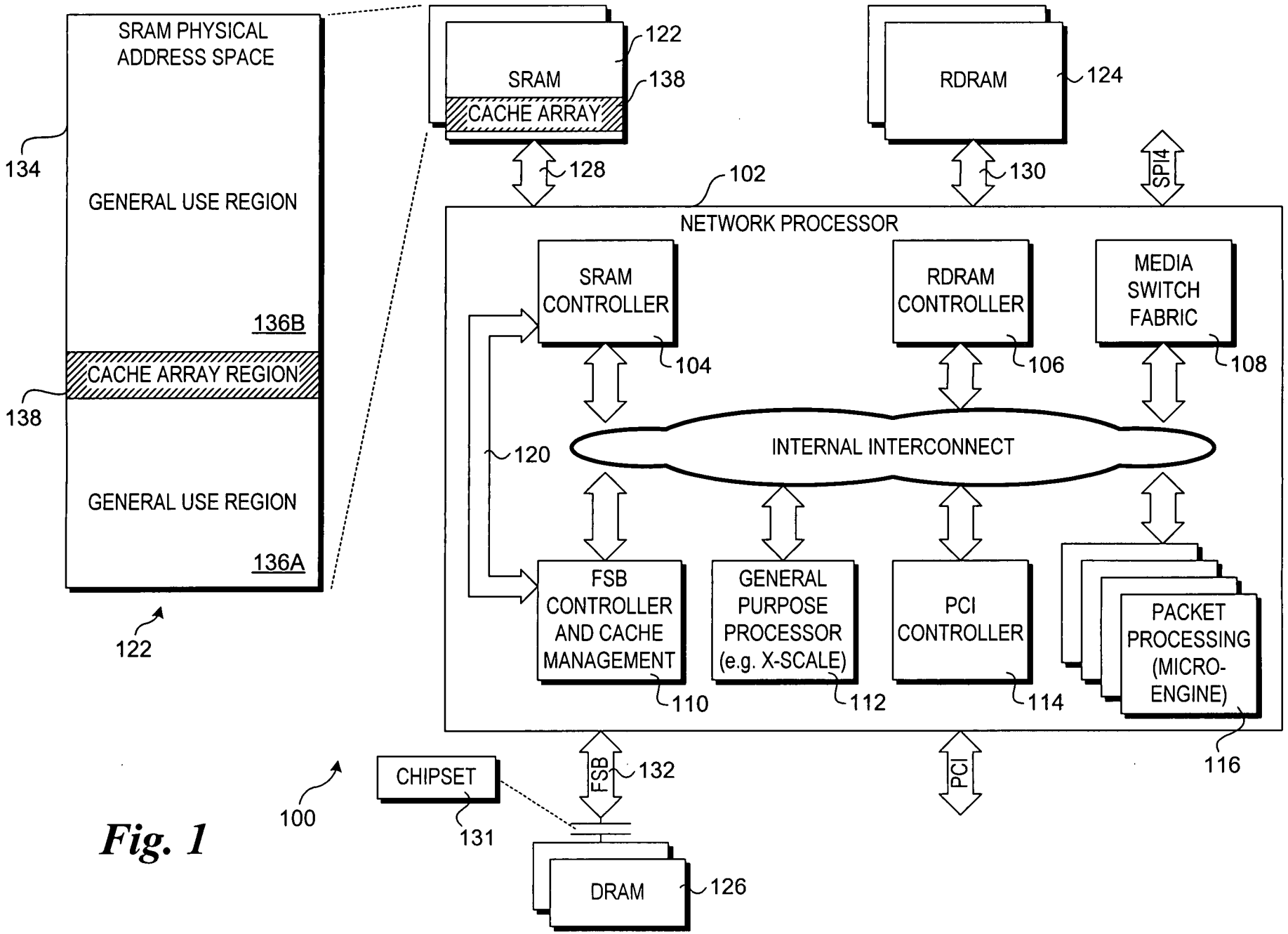

SRAM PHYSICAL ADDRESS SPACE
134
GENERAL USE REGION
136B
CACHE ARRAY REGION
138
GENERAL USE REGION
136A
122
SRAM
CACHE ARRAY
122
138
128
RDRAM
124
130
SPI4
102
NETWORK PROCESSOR
SRAM CONTROLLER
104
RDRAM CONTROLLER
106
MEDIA SWITCH FABRIC
108
120
INTERNAL INTERCONNECT
FSB CONTROLLER AND CACHE MANAGEMENT
110
GENERAL PURPOSE PROCESSOR (e.g. X-SCALE)
112
PCI CONTROLLER
114
PACKET PROCESSING (MICRO-ENGINE)
116
FSB
132
PCI
CHIPSET
131
100
DRAM
126

Fig. 1

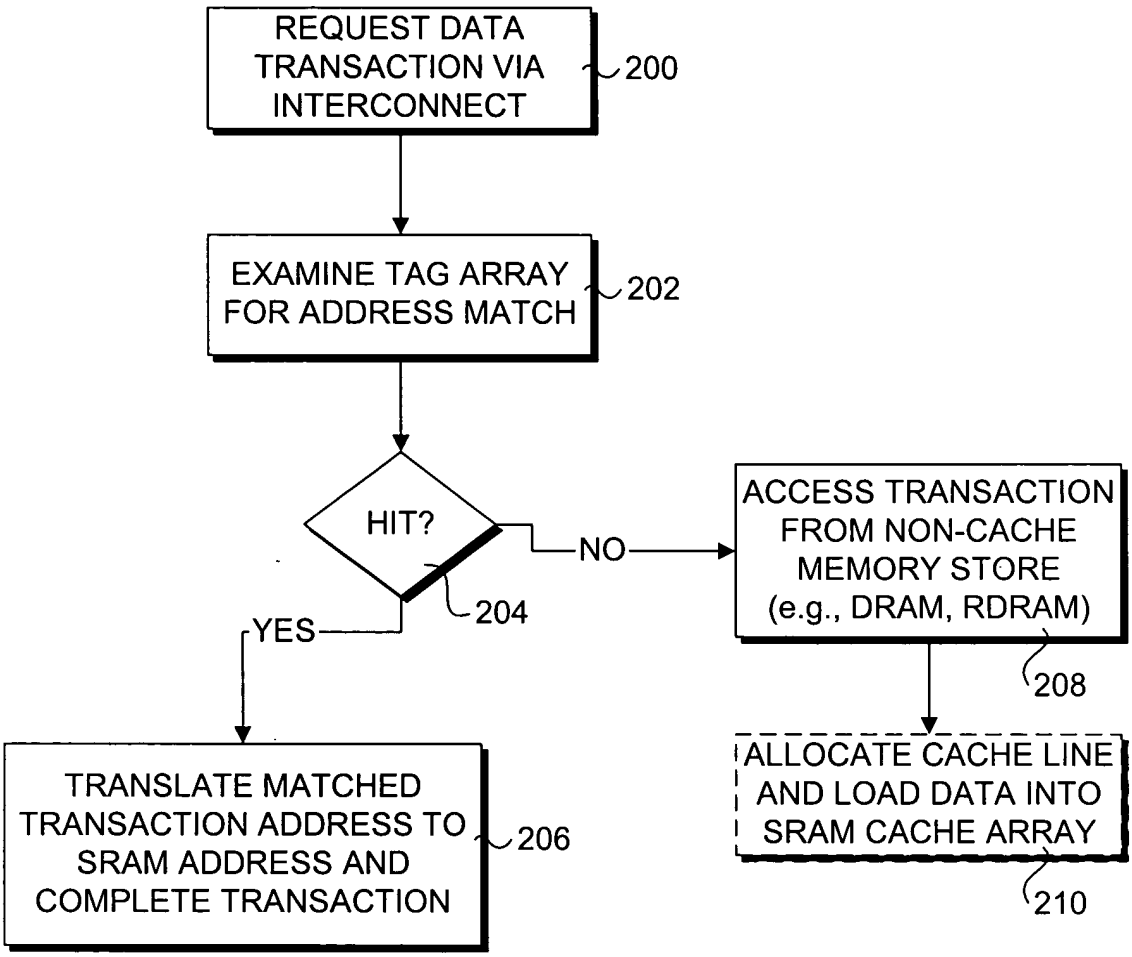

REQUEST DATA TRANSACTION VIA INTERCONNECT
200
EXAMINE TAG ARRAY FOR ADDRESS MATCH
202
HIT?
204
NO
YES
ACCESS TRANSACTION FROM NON-CACHE MEMORY STORE (e.g., DRAM, RDRAM)
208
ALLOCATE CACHE LINE AND LOAD DATA INTO SRAM CACHE ARRAY
210
TRANSLATE MATCHED TRANSACTION ADDRESS TO SRAM ADDRESS AND COMPLETE TRANSACTION
206

Fig. 2

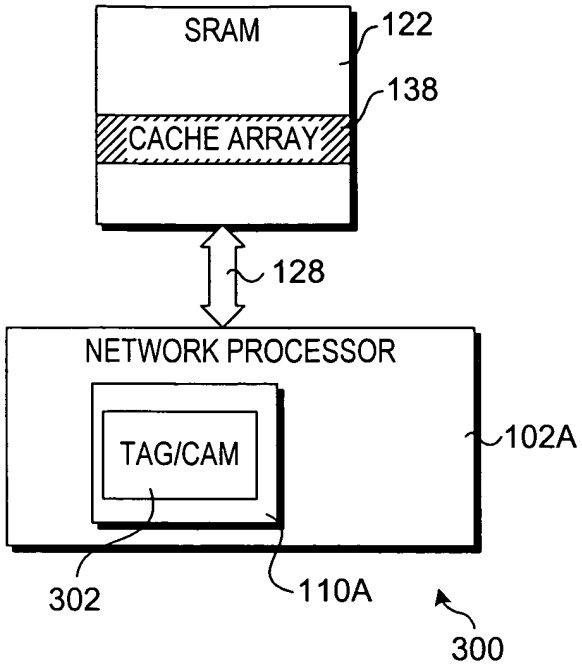

SRAM
122
138
CACHE ARRAY
128
NETWORK PROCESSOR
TAG/CAM
102A
302
110A
300

Fig. 3

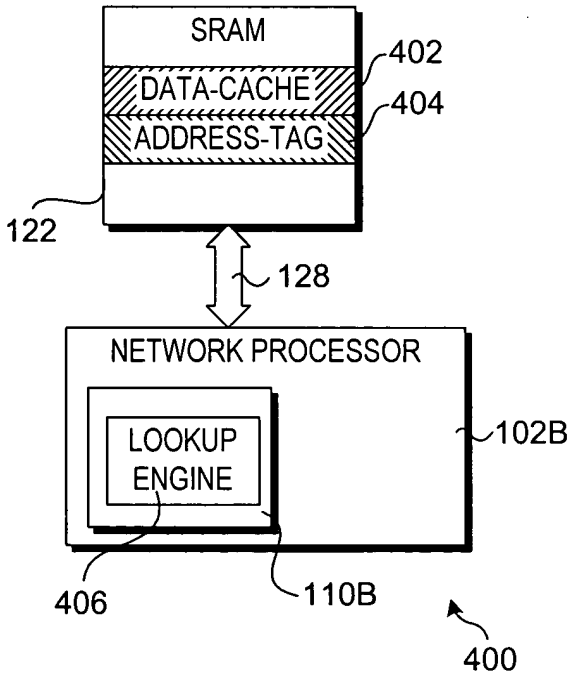
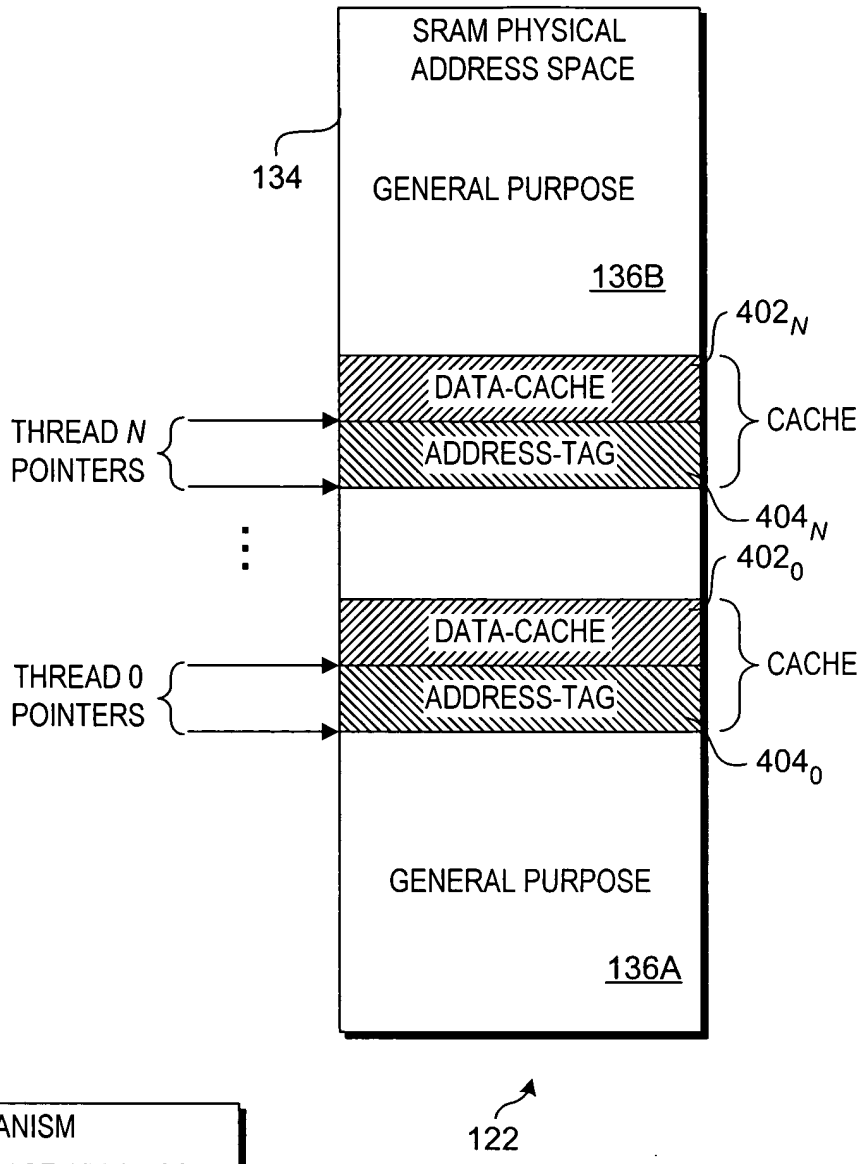

SRAM
402
DATA-CACHE
404
ADDRESS-TAG
122
128
NETWORK PROCESSOR
LOOKUP ENGINE
102B
406
110B
400

Fig. 4

Fig. 5a



MAPPING MECHANISM

THREAD 0:	T0 - ADDR TAG BASE ADDRESS
	T0 - DATA CACHE BASE ADDRESS
THREAD 1:	T1 - ADDR TAG BASE ADDRESS
	T1 - DATA CACHE BASE ADDRESS
THREAD 2:	T2 - ADDR TAG BASE ADDRESS
	T2 - DATA CACHE BASE ADDRESS
THREAD *N*:	T*N* - ADDR TAG BASE ADDRESS
	T*N* - DATA CACHE BASE ADDRESS

500

Fig. 5b

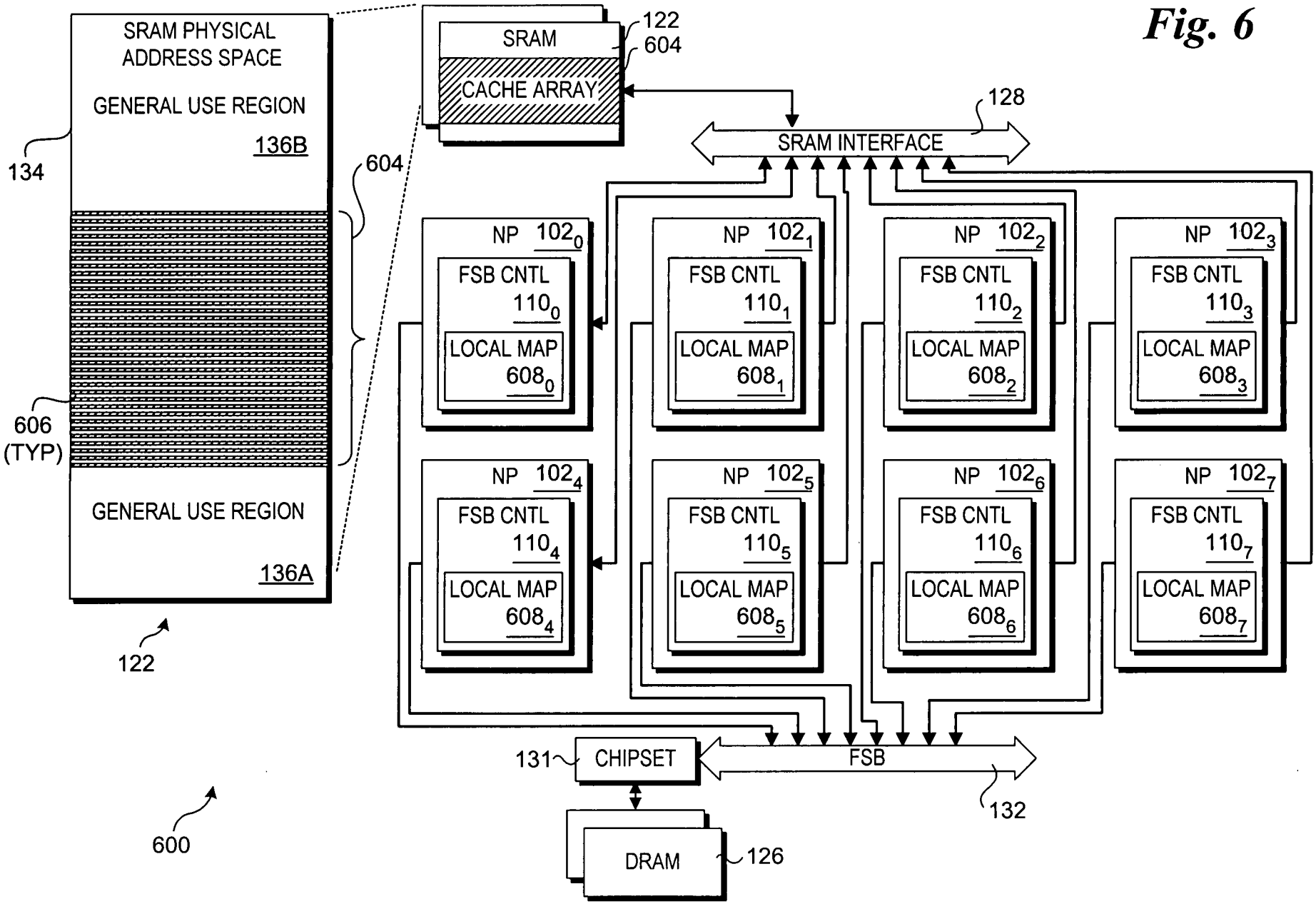

SRAM PHYSICAL ADDRESS SPACE
GENERAL USE REGION
136B
134
604
606 (TYP)
GENERAL USE REGION
136A
122
600
SRAM
CACHE ARRAY
122
604
128
SRAM INTERFACE
NP 102$_0$
FSB CNTL 110$_0$
LOCAL MAP 608$_0$
NP 102$_1$
FSB CNTL 110$_1$
LOCAL MAP 608$_1$
NP 102$_2$
FSB CNTL 110$_2$
LOCAL MAP 608$_2$
NP 102$_3$
FSB CNTL 110$_3$
LOCAL MAP 608$_3$
NP 102$_4$
FSB CNTL 110$_4$
LOCAL MAP 608$_4$
NP 102$_5$
FSB CNTL 110$_5$
LOCAL MAP 608$_5$
NP 102$_6$
FSB CNTL 110$_6$
LOCAL MAP 608$_6$
NP 102$_7$
FSB CNTL 110$_7$
LOCAL MAP 608$_7$
131
CHIPSET
FSB
132
DRAM
126

Fig. 6

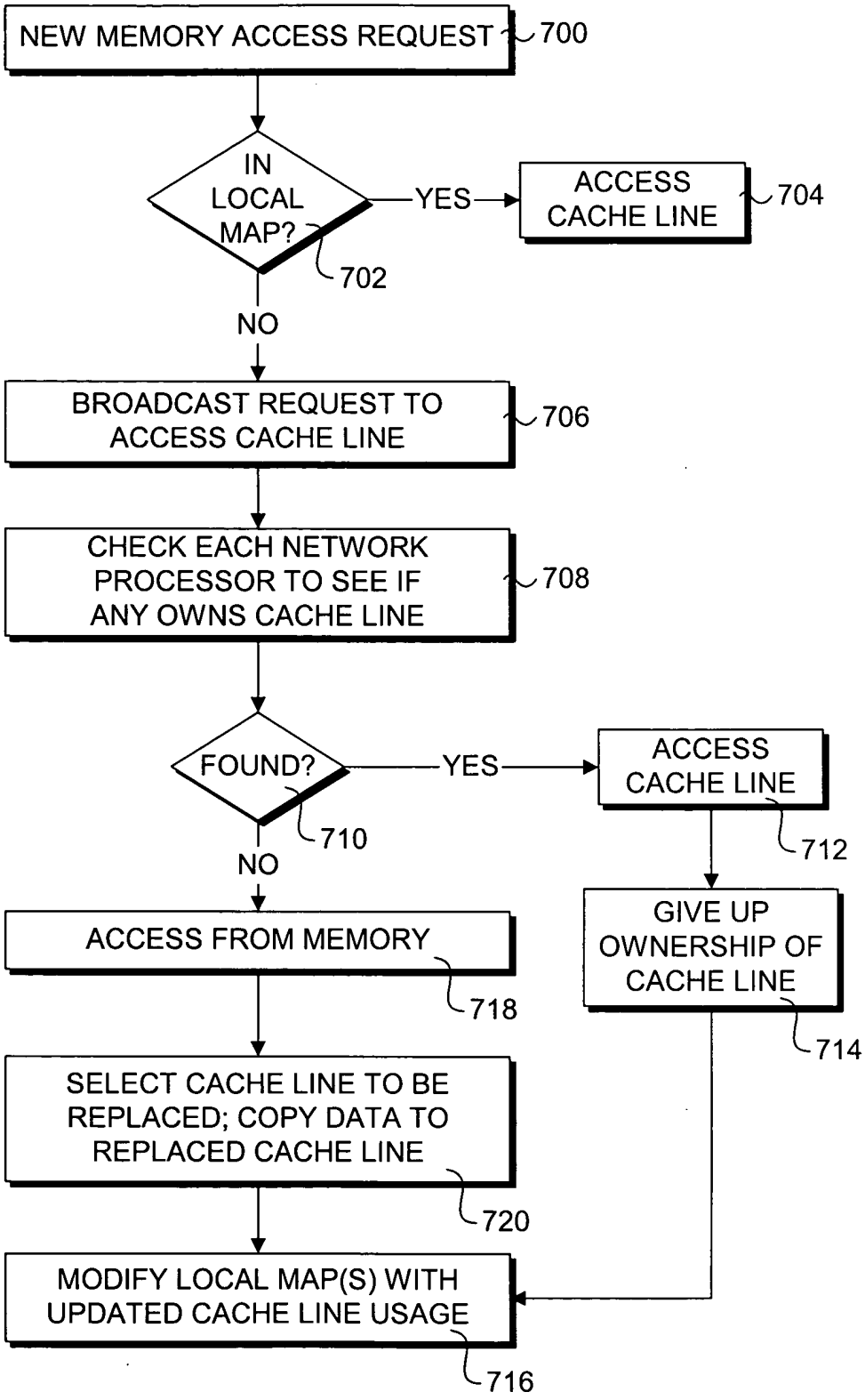

NEW MEMORY ACCESS REQUEST
700
IN LOCAL MAP?
YES
ACCESS CACHE LINE
704
702
NO
BROADCAST REQUEST TO ACCESS CACHE LINE
706
CHECK EACH NETWORK PROCESSOR TO SEE IF ANY OWNS CACHE LINE
708
FOUND?
YES
ACCESS CACHE LINE
710
712
NO
GIVE UP OWNERSHIP OF CACHE LINE
714
ACCESS FROM MEMORY
718
SELECT CACHE LINE TO BE REPLACED; COPY DATA TO REPLACED CACHE LINE
720
MODIFY LOCAL MAP(S) WITH UPDATED CACHE LINE USAGE
716

Fig. 7